In the Claims

Please add new Claims 28-46.

28. (New)A data encryption system comprising:

a control process which modifies a received packet to include control data which identifies processes to be performed on the packet;

a plurality of processors which perform the processes identified by the control data, including an encryption process;

an interconnection which responds to control data in the packet to forward the packet with control data from processor to processor; and

an output from which the processed packet is forwarded without the control data.

29. (New)The system as claimed in Claim 28 wherein the interconnection comprises a packet buffer including a buffer controller which determines a next processor of the plurality of processors to process the data packet.

30. (New)The system as claimed in Claim 29 wherein the buffer controller includes a resource manager which maintains information on resource processor availability.

31. (New)The system as claimed in Claim 28 wherein the control data includes code to be processed in at least one of the processors.

32. (New)The system as claimed in Claim 28 wherein the control data further includes an encryption or authentication key.

33. (New)The system as claimed in Claim 28 wherein individual processors add result data to the control data.

34. (New)The system as claimed in Claim 28 wherein the processors perform IPSEC protocol processing.

35. (New)The system as claimed in Claim 28 wherein respective processors perform IP header manipulation and encryption.

36. (New)The system as claimed in Claim 35 wherein a processor performs authentication processing.

37. (New)A method of encrypting or decrypting data packets comprising:

modifying a received packet to include control data which identifies processes to be performed on the packet; and

in successive processors, performing the processes identified by the control data, including an encryption or decryption process.

38. (New)The method as claimed in Claim 37 wherein the packet is forwarded from processor to processor through an interconnection which responds to control data in the packets.

39. (New)The method as claimed in Claim 38 wherein the interconnection comprises a packet buffer including a buffer controller which determines a next processor of the plurality of processors to process the data packet.

40. (New)The method as claimed in Claim 37 wherein the buffer controller includes a resource manager which maintains information on resource processor availability.

41. (New)The method as claimed in Claim 37 wherein the control data includes code to be processed in at least one of the processors.

42. (New)The method as claimed in Claim 37 wherein the control data further includes an